

Amendments to the Specification:

Please replace paragraph [0015] with the following amended paragraph:

[0015] Referring to Fig. 2b, the sacrificial layer is patterned using a photoresist process, and some area on which an MIM capacitor is formed is removed by dry-etch or wet-etch. Then, an upper metal layer 15[[4]] and a dielectric layer 14[[5]] are deposited in sequence. The dielectric layer is formed by chemical vapor deposition or atomic layer deposition using a material such as SiN, SiO₂, Al₂O₃, TaON, TiO₂, Ta₂O₅, ZrO₂, (Ba,Sr)TiO₃ (hereinafter referred to as “BST”), (Pb,Zr)TiO₃ (hereinafter referred to as “PZT”), or (Pb,La)(Zr,Ti)O₃ (hereinafter referred to as “PLZT”). The dielectric layer is a single layer or multi-layer with a thickness of 200~1000Å.